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10/025,851	12/26/2001	Jeong Il Bang	HI-0066	7554
34610	7590	06/13/2005	EXAMINER	
FLESHNER & KIM, LLP P.O. BOX 221200 CHANTILLY, VA 20153			CHU, GABRIEL L	
			ART UNIT	PAPER NUMBER
			2114	

DATE MAILED: 06/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/025,851

Applicant(s)

BANG, JEONG IL

Examiner

Gabriel L. Chu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 26 December 2001.  
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-19 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-19 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Claim Objections***

1. Claims 8, 15, 18 objected to because of the following informalities:

Referring to claim 8, "checking an operation region of a current task being accessed and outputting a result" is not clear. It is understood to refer to "checking an operation region being accessed by a current task and outputting a result".

Referring to claim 15, "A apparatus" is properly "An apparatus".

Referring to claim 18, "the address signal" has no antecedent basis. It is understood to refer to "an address signal".

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 1-19 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Referring to claims 1-19, the independent claims, and particularly claims 8 and 18, claim a method/apparatus for "generating an interrupt signal when the task is performed in a region other than the designated region". In the specification, the *only* manner in which this can be accomplished is described in paragraphs [0028] to [0029] and again in

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paragraphs [0034] to [0035], in further view of figure 5. The method outlined in these paragraphs require the use of address, WR, and Task N signals whose identity, purpose, and contents have not been sufficiently described so as one of ordinary skill in the art may understand their purpose in determining whether or not to generate an interrupt/grant signal. As this information is considered critical to the enablement of the invention, it is also considered essential, see rejection below.

4. Claims 1-19 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. The means by which the invention “determines if the task is not being performed in the designated region” is considered critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

Paragraphs [0027] and [0034]-[0035] describe as essential steps “determining if a task is performed in a designated region”, but do not describe the manner by which this is accomplished. Further, as a result of this determination, and further considered critical to the practice of this invention, an address is generated or not generated that is used in a comparison to determine whether an interrupt is generated or not. As outlined in the independent claims 1, 10, and 15, this interrupt generation method/apparatus is considered to be the crux of the invention, and therefore subject matter considered to be crucial to the implementation of this method/apparatus has not been disclosed in the specification or claims.

More specifically, although it is understood and disclosed at least in limitation (b) of claim 10 wherein “checking an operation region of a task that is accessed based on

an access of data" may allude to an access address and that a designated region may comprise a range of designated addresses, this information alone does not solve the puzzle that is figure 5. In figure 5, the generated address (see paragraph [0035]) is input in part, and in part input as a single line (see A9 & A8). No explanation of the meaning of the address data is given. Crucially, the data values for these address bits may provide a clue as to why the value of the address is important in determining comparison for generating an interrupt/grant.

Further confounding interpretation is the presence of WR and "Task N" signals. WR is described in [0028], "As shown in FIG. 3, the task signal can be inputted into one of the task comparing units (e.g., 48c), and that task comparing unit can output a grant signal according to the address signal inputted based on the task signal. As shown in FIG. 3, instead of the grant signal, a write signal (WR) that is generated from the central processing unit 10 can be used instead. If the write signal (WR) is a prescribed value such as `1`, the write signal (WR) is a read signal, and if the write signal (WR) is set to `0`, the write signal (WR) is a write signal. However, it should be noted that the grant signal output is dependent or preferably totally dependent on the address signal. The address signal is preferably a signal for indicating whether a task is performed in the designated area or not." In figure 3, no WR signal is shown, however WR is shown in figure 5. Paragraph [0028] clearly says that a CPU can generate a WR signal instead of a grant signal and yet from all other indications, the grant signal is generated from comparing units (or the task testing unit). Further, WR is not output *instead* of a grant signal, it is apparently, according to figure 5, *input* into an AND gate as part of the

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comparison to determine whether or not to generate a grant signal. Further, no indication is made of what the write/read signal WR enables writes or reads.

In paragraph [0029], "Therefore, the task comparing unit (e.g., 48c) can generate the grant signal having prescribed values such as `0` or `1`, in accordance with the consequence of the address signal and based on both the task signal and the write signal (WR). At this time, if the grant signal `0` is generated, which preferably means that the task is not performed in the designated region, an interrupt signal can be generated." From paragraph [0025], "In addition, in order to perform the task, the central processing unit 10 preferably sends a task ID enable signal out to the task testing unit 40, and generates a data signal corresponding to the task ID, simultaneously. The data signal is a binary combination that can determine or identify the task ID. For example, if the task ID is 3, the data signal can be generated as `0011` from the most significant bits of a data bus." Examiner can only assume that this data signal is somehow related to the "task signal". In figure 5, "Task N" appears to be a single bit, which would make sense in light of the AND gate it is fed into. Regardless, it is not clear why a task signal is used in determining a grant/interrupt generation.

### ***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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6. Claims 1-7 and 10-17 rejected under 35 U.S.C. 102(b) as being anticipated by US 5113521 to McKeen et al. Referring to claim 1, McKeen discloses a method for debugging in an application program, the method comprising:

writing information on a task to be performed (From line 29 of column 14, "Associated with each vector register involved in executing a vector instruction is one of several counters 44 in vector register control logic 60 which counts down from n to 0 as the suboperations are being performed, and which provides an address for the associated vector elements in the associated vector register. If a vector instruction is stopped due to a memory management exception, the value of one of the counters 44 associated with the faulting instruction indicates the suboperation at which the exception occurred. That value, as well as the counter associated with any other unfinished instruction, is preferably stored as part of VPU 30 state information. When VPU 30 is reloaded with the stored state information, and the memory management fault is called, counters 44 are reloaded with the suboperation values so the execution of the faulting instruction and all unfinished instructions can begin where the exception occurred. This hardware is shown in greater detail in U.S. Ser. No. 093,499, which is herein incorporated by reference.");

checking whether the task is performed in a designated region; and generating an interrupt signal when the task is performed in a region other than the designated region for the task (From line 34 of column 14, "If a vector instruction is stopped due to a memory management exception...").

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7. Referring to claim 2, McKeen discloses the information on the task is a task identifier (From line 29 of column 14, "Associated with each vector register involved in executing a vector instruction is one of several counters 44 in vector register control logic 60 which counts down from n to 0 as the suboperations are being performed, and which provides an address for the associated vector elements in the associated vector register.").

8. Referring to claim 3, McKeen discloses latching a data signal corresponding to the written information on the task (From line 29 of column 14, "Associated with each vector register involved in executing a vector instruction is one of several counters 44 in vector register control logic 60 which counts down from n to 0 as the suboperations are being performed, and which provides an address for the associated vector elements in the associated vector register. . If a vector instruction is stopped due to a memory management exception, the value of one of the counters 44 associated with the faulting instruction indicates the suboperation at which the exception occurred.");

and outputting a task signal corresponding to the task identifier that is identified based on the latched data signal (From line 41 of column 14, "When VPU 30 is reloaded with the stored state information, and the memory management fault is called, counters 44 are reloaded with the suboperation values so the execution of the faulting instruction and all unfinished instructions can begin where the exception occurred.").

9. Referring to claim 4, 13, McKeen discloses the designated region is an operation region assigned to each task (From line 37 of column 12, "Access control violations



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involve attempts by VPU 30 to access protected portions of memory or portions of memory outside of the memory space allocated to the current vector process.”).

10. Referring to claim 5, McKeen discloses determining the information on the task responsive to the interrupt signal (From line 34 of column 14, “If a vector instruction is stopped due to a memory management exception, the value of one of the counters 44 associated with the faulting instruction indicates the suboperation at which the exception occurred. That value, as well as the counter associated with any other unfinished instruction, s preferably stored as part of VPU 30 state information. When VPU 30 is reloaded with the stored state information, and the memory management fault is called, counters 44 are reloaded with the suboperation values so the execution of the faulting instruction and all unfinished instructions can begin where the exception occurred.”);

and performing an operation corresponding to the information on the task based on the determination (From line 44 of column 14, “execution of the faulting instruction and all unfinished instructions can begin where the exception occurred.”).

11. Referring to claim 6, McKeen discloses sending a control signal that is generated based on the interrupt signal to a memory (From line 41 of column 14, “When VPU 30 is reloaded with the stored state information, and the memory management fault is called, counters 44 are reloaded with the suboperation values so the execution of the faulting instruction and all unfinished instructions can begin where the exception occurred.”).

12. Referring to claim 7, McKeen discloses after a task switching occurs to a next task (From line 29 of column 14, “Associated with each vector register involved in executing a vector instruction is one of several counters 44 in vector register control

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logic 60 which counts down from n to 0 as the suboperations are being performed, and which provides an address for the associated vector elements in the associated vector register.”), a checking process based on information corresponding to the next task is repeatedly conducted to check whether the next task is performed in a corresponding designated region (From line 34 of column 14, “If a vector instruction is stopped due to a memory management exception, the value of one of the counters 44 associated with the faulting instruction indicates the suboperation at which the exception occurred.” Wherein the exception can occur for any suboperation.).

13. Referring to claim 10, McKeen discloses a method for debugging in an application program, the method comprising:

(a) outputting a task signal corresponding to a task identifier that is identified based on a data signal corresponding to the task identifier (From line 29 of column 14, “Associated with each vector register involved in executing a vector instruction is one of several counters 44 in vector register control logic 60 which counts down from n to 0 as the suboperations are being performed, and which provides an address for the associated vector elements in the associated vector register. If a vector instruction is stopped due to a memory management exception, the value of one of the counters 44 associated with the faulting instruction indicates the suboperation at which the exception occurred. That value, as well as the counter associated with any other unfinished instruction, is preferably stored as part of VPU 30 state information. When VPU 30 is reloaded with the stored state information, and the memory management fault is called, counters 44 are reloaded with the suboperation values so the execution of the faulting

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instruction and all unfinished instructions can begin where the exception occurred. This hardware is shown in greater detail in U.S. Ser. No. 093,499, which is herein incorporated by reference.”);

(b) checking an operation region of a task that is accessed based on an access of data; (c) judging whether the task is performed in a designated region based on an address signal corresponding to a result of the checking; and (d) generating an interrupt signal when the task is not performed in the designated region as a result of the judging (From line 34 of column 14, “If a vector instruction is stopped due to a memory management exception, the value of one of the counters 44 associated with the faulting instruction indicates the suboperation at which the exception occurred.”).

14. Referring to claim 11, McKeen discloses when a task switching occurs, the steps (a) through (d) are repeatedly performed based on a next task identifier (From line 34 of column 14, “If a vector instruction is stopped due to a memory management exception, the value of one of the counters 44 associated with the faulting instruction indicates the suboperation at which the exception occurred.” Wherein the exception can occur for any suboperation.).

15. Referring to claim 12, McKeen discloses the task identifier is provided for each task to be performed, and wherein the task identifier is selectably stored for said each task (From line 29 of column 14, “Associated with each vector register involved in executing a vector instruction is one of several counters 44 in vector register control logic 60 which counts down from n to 0 as the suboperations are being performed, and

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which provides an address for the associated vector elements in the associated vector register.”).

16. Referring to claim 14, McKeen discloses the task signal is used for generating the interrupt signal (From line 29 of column 14, “Associated with each vector register involved in executing a vector instruction is one of several counters 44 in vector register control logic 60 which counts down from n to 0 as the suboperations are being performed, and which provides an address for the associated vector elements in the associated vector register.” Wherein the suboperation access violations result in exceptions.).

17. Referring to claim 15, McKeen discloses an apparatus for debugging in an application program, the apparatus comprising:

first control means for writing a task identifier provided for each task to be performed, for generating a data signal corresponding to the task identifier, and for activating a selected task (From line 29 of column 14, “Associated with each vector register involved in executing a vector instruction is one of several counters 44 in vector register control logic 60 which counts down from n to 0 as the suboperations are being performed, and which provides an address for the associated vector elements in the associated vector register.”);

task checking means for outputting a task signal corresponding to the task identifier that is identified based on the data signal, and for generating an interrupt signal according to a determination whether a current task is performed in a designated region (From line 34 of column 14, “If a vector instruction is stopped due to a memory

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management exception, the value of one of the counters 44 associated with the faulting instruction indicates the suboperation at which the exception occurred.”);

and storage means for writing the task identifier provided by the first control means, and for assigning an operation region to each task (From line 29 of column 14, “Associated with each vector register involved in executing a vector instruction is one of several counters 44 in vector register control logic 60 which counts down from n to 0 as the suboperations are being performed, and which provides an address for the associated vector elements in the associated vector register.” From line 37 of column 12, “Access control violations involve attempts by VPU 30 to access protected portions of memory or portions of memory outside of the memory space allocated to the current vector process.”).

18. Referring to claim 16, McKeen discloses second control means for outputting a control signal to control the storage means based on the generated interrupt signal (From line 41 of column 14, “When VPU 30 is reloaded with the stored state information, and the memory management fault is called, counters 44 are reloaded with the suboperation values so the execution of the faulting instruction and all unfinished instructions can begin where the exception occurred.”).

19. Referring to claim 17, McKeen discloses an address signal is used as a basis of determining whether the current task is performed in the designated region (From line 37 of column 12, “Access control violations involve attempts by VPU 30 to access protected portions of memory or portions of memory outside of the memory space allocated to the current vector process. The current vector process refers to the

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process containing the vector instruction whose execution caused the memory management exception." Wherein determining what is or is not in a memory space involves addresses.).

20. It is noted that claims 8, 9, 18, and 19 are not specifically addressed by an art rejection for reasons noted above in 112 rejections.

### ***Conclusion***

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 2001/0021966 to Kawasaki et al.

US 5193180 to Hastings

US 5644709 to Austin

US 6634020 to Bates et al.

US 6658653 to Bates et al.

US 6697971 to Dwyer

US 6728907 to Wang et al.

US 6745344 to Joshi et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (571) 272-3656. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel, Jr. can be reached on (571) 272-3645. The fax

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phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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